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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,564	03/04/2005	Takumi Yamaguchi	67471-065	9368

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EXAMINER	
LIU, BENJAMIN T	
ART UNIT	**PAPER NUMBER**
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,564	YAMAGUCHI, TAKUMI	
	Examiner	Art Unit	
	Benjamin T. Liu	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/13/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claim 1-14 is hereby withdrawn due to the newly cited reference Kurosawa et al. (2001/0052574) provided by applicant on the 13 February 2007. Rejections based on the newly cited reference follow. Since the IDS was filed under 37 CFR 1.97(d), this action is not made final.

Specification

2. The disclosure is objected to because of the following informalities:

In every instance in the abstract and specification where applicant writes "shift resistor" should be replaced with –shift register—for clarity.

Appropriate correction is required.

Claim Objection

3. Claim 4 is objected to because of the following informalities:

In claim 4, line 4, "shift resistor" should be changed to –shift register—for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-5 and 10-11 are rejected under 35 U.S.C 102(a) as being anticipated by Kurosawa et al. (2001/0052574).

With regard to claims 1 and 10, figures 4 and 12 of Kurosawa et al. disclose a solid-state imaging apparatus that includes an imaging region 11 and a drive circuit region 15; the imaging region 11 including the active-type unit pixels 180 which are arranged in rows and columns, wherein each active-type unit pixel 180 comprising a photodiode unit 132 generates signal charge by photoelectric conversion and an amplification unit 133 amplifies the signal charge; the drive circuit region 15 comprising plurality of readout circuits 260, each being for driving the photodiode unit 132 and the amplification unit 133 of the corresponding active-type unit pixel 180; the active-type unit pixels 180 of the imaging region 11 and the readout circuits 260 of the drive circuit region 15 including plurality of transistors respectively, wherein all the transistors of the active-type unit pixels 180 in the imaging region 11 and all the transistors of the readout circuits 260 of the drive circuit region 15 have a same channel polarity (i.e. N-channel transistor). Note that claim 1 and claim 10 do not recite the driving region comprising a time generation circuit, a vertical shift register circuit and a horizontal shift register circuit wherein all the transistors of these circuits are the same channel polarity as that of the active-type unit pixels 180 in the imaging region 11, therefore claims 1 and 10 do not distinguish over Kurosawa et al. Further, it is inherent that the imaging region 11 and the drive circuit region 15 of Kurosawa et al. are formed on one semiconductor substrate, because the imaging apparatus regions need to form on a support substrate.

With regard to claims 2 and 11, figure 12 of Kurosawa et al. discloses all the transistors 131, 133, 182, 134 of each active-type unit pixel 180 of the imaging region 11 and all the transistors 261, 265, 269, 268 of each readout circuit 260 of the drive circuit region 15 are of an n-channel MOS type. Note paragraphs [0043] and [0056] of Kurosawa et al.

With regard to claim 3, figure 12 of Kurosawa et al. discloses each readout circuit 260 of the drive circuit region 15 includes a dynamic circuit that includes a capacitor 263 for accumulating electric charge and a transistor 265 for performing a switching function.

With regard to claim 4, figures 4 and 12 of Kurosawa et al. disclose the imaging region 11 includes a plurality of active-type unit pixels 180, and the drive circuit region 15 includes a plurality of readout circuits 260 each comprising a pixel selection circuit 265 for selecting one active-type unit pixel 180 from the plurality of active-type unit pixels 180, and a shift register circuit 14 for outputting a selection instruction signal to the pixel selection circuit 265 of the readout circuit 260.

With regard to claim 5, figure 12 of Kurosawa et al. discloses the active-type unit pixel 180 of the imaging region 11 includes a transistor 182 for performing a switching function based on a signal received from the drive circuit region 260, and the signal charge is output to the amplification unit 133 while the transistor for performing the switching function is ON.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8 and 12-14 are rejected under 35 U.S.C 103(a) as being unpatentable over Kurosawa et al. (2001/0052574) in view of Momose et al. (6,642,560).

With regard to claims 6 and 12, figures 4 and 12 of Kurosawa et al. disclose all the subject matter claimed except for a gate length of each MOS transistor is equal to or less than 0.6 μm.

However, figure 1 and lines 19-23 in column 6 of Momose et al. disclose a MOS transistor having a gate length Lg is less than 0.6 μm (i.e. equal to or less than 0.3 μm.)

Therefore, it would have been obvious to one of ordinary skill in the art to form the MOS transistors of Kurosawa et al. each having a gate length Lg is equal to or less than 0.6 μm such as taught by Momose et al. in order to decrease the size of the MOS transistors while reducing the gate leakage current. Note the abstract of Momose et al.

With regard to claims 7 and 13, Kurosawa et al. discloses all the subject matter claimed except for a gate insulator of each MOS transistor having a thickness is in a range of 1 nm to 20 nm.

However, figure 1 and lines 19-23 in column 6 of Momose et al. disclose a MOS transistor having a gate insulator 3 having a thickness of less than 2.5nm, which is in a range from 1 nm to 20 nm.

Therefore, it would have been obvious to one of ordinary skill in the art to form the MOS transistors of Kurosawa et al. each having gate insulator thickness is in a range of 1 nm to 20 nm such as taught by Momose et al. in order to maintain a certain threshold voltage in each transistor.

With regard to claims 8 and 14, Kurosawa et al. disclose all the subject matter claimed except for each MOS transistor having an insulator that has a film thickness in a range from 1 nm to 20 nm and functions as a capacitor, which is formed between a gate electrode of the transistor and the semiconductor substrate.

However, figure 1 and lines 19-23 in column 6 of Momose et al. disclose a MOS transistor having an insulator 3 that has a film thickness of less than 2.5nm, which is in a range from 1nm to 20nm. It is inherent that the insulator 3 of the MOS transistor of Momose et al. functions as a capacitor that is formed between a gate electrode 2 and the semiconductor substrate 1, because the insulator 3 is formed between two conductive layers 2 and 1.

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Kurosawa et al. having the transistors such as taught by Momose et al. in order to maintain a certain threshold voltage in each transistor.

Claim 9 is rejected under 35 U.S.C 103(a) as being unpatentable over Kurosawa et al. (2001/0052574) in view of Shinohara et al. (5,698,844).

With regard to claim 9, figures 4 and 12 of Kurosawa et al. disclose all the subject matter claimed except for a camera that includes the solid-state imaging apparatus.

However, lines 8-10 in column 1 of Shinohara et al. disclose a solid-state imaging apparatus can be included in a camera.

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the solid-state imaging apparatus of Kurosawa et al. in the camera such as taught by Shinohara et al. in order to form line sensors for an image scanner and an area sensor for the camera.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin T. Liu whose telephone number is (571) 272-6009. The examiner can normally be reached on Mon-Fri 9:30 AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTL
3/8/07